PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification:
H01L 29/43, H01L 21/441

A1

(11) International Publication Number: WO 00/11721

(43) International Publication Date: 02 March 2000 (02.03.2000)

(21) International Application Number: PCT/US99/16719

(22) International Filing Date: 18 August 1999 (18.08.1999)

(30) Priority Data:

09/137,083	20 August 1998 (20.08.1998)	US
09/137,084	20 August 1998 (20.08.1998)	US
09/137,085	20 August 1998 (20.08.1998)	US
09/137,086	20 August 1998 (20.08.1998)	US
09/137,087	20 August 1998 (20.08.1998)	US
09/137,088	20 August 1998 (20.08.1998)	US
09/137,089	20 August 1998 (20.08.1998)	US
09/215,127	18 December1998 (18.12.1998)	US
09/215,128	18 December1998 (18.12.1998)	US

Published

(60) Parent Application or Grant
THE GOVERNMENT OF THE UNITED STATES OF AMERICA, represented by THE SECRETARY OF THE NAVY [/]; (). STUMBORG, Michael, F. [/]; (). SANTIAGO, Francisco [/]; (). CHU, Tak-Kin [/]; (). BOULAIS, Kevin, A. [/]; (). BECHTEL, James, B. ; ().

(54) Title: ELECTRONIC DEVICES WITH BARRIER FILM AND PROCESS FOR MAKING SAME

(54) Titre: DISPOSITIFS ELECTRONIQUES POURVUS DE FILMS BARRIERES ET PROCEDE DE FABRICATION

(57) Abstract

A semiconductor device having a barrier film (47) comprising an extremely thin film formed of one or more monolayers each comprised of a two-dimensional array of metal atoms. In one exemplary aspect, the barrier film (47, 49) is used for preventing the diffusion of atoms of another material (45) such as copper conductor, into a substrate (46), such as a semiconducting material or an insulating material, and an oxide layer (48). Methods for making the barrier film (47) in a semiconductor device are also covered. The extremely thin barrier film (47, 49) makes possible a significant increase in the component density and a corresponding reduction in the number of layers in large scale integrated circuits, as well as improved performance.

(57) Abrégé

Ce dispositif à semi-conducteurs est pourvu d'un film barrière (47), constitué d'une pellicule extrêmement mince formée d'une monocouche, sinon de plusieurs, faites, chacune, d'un réseau bi-dimensionnel d'atomes de métal. Dans un mode de réalisation, donné à titre d'exemple, on utilise le film barrière (47, 49) pour empêcher la diffusion d'atomes d'une autre matière (45), un conducteur en cuivre notamment, dans un substrat (46), tels qu'un matériau semi-conducteur ou isolant, et dans une couche d'oxyde (48). L'invention a également trait à des procédés de fabrication de ce film barrière (47) dans un dispositif à semi-conducteurs. La présence de ce film barrière extrêmement mince (24, 54) permet d'accroître la densité du composant et de réduire, de façon corollaire, le nombre de couches dans des circuits intégrés de grande taille ainsi que d'améliorer les caractéristiques de fonctionnement.

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 29/43, 21/441

A1

(11) International Publication Number: WO 00/11721

(43) International Publication Date: 2 March 2000 (02.03.00)

(21) International Application Number: PCT/US99/16719

(22) International Filing Date: 18 August 1999 (18.08.99)

(30) Priority Data:

09/137,083	20 August 1998 (20.08.98)	US
09/137,084	20 August 1998 (20.08.98)	US
09/137,085	20 August 1998 (20.08.98)	US
09/137,086	20 August 1998 (20.08.98)	US
09/137,087	20 August 1998 (20.08.98)	US
09/137,088	20 August 1998 (20.08.98)	US
09/137,089	20 August 1998 (20.08.98)	US
09/215,127	18 December 1998 (18.12.98)	US
09/215,128	18 December 1998 (18.12.98)	US

(71) Applicant: THE GOVERNMENT OF THE UNITED STATES OF AMERICA, represented by THE SECRETARY OF THE NAVY [US/US]; Naval Surface Warfare Center, Dahlgren Division, Dahlgren, VA 22448 (US).

(72) Inventors: STUMBORG, Michael, F.; 201 Progress Street, Fredericksburg, VA 22401 (US). SANTIAGO, Francisco; 5308 Cedar Ridge Drive, Fredericksburg, VA 22407 (US). CHU, Tak-Kin; 9506 Nowell, Bethesda, MD 20817 (US). BOULAIS, Kevin, A.; 1315 Wilson, Waldorf, MD 20602 (US).

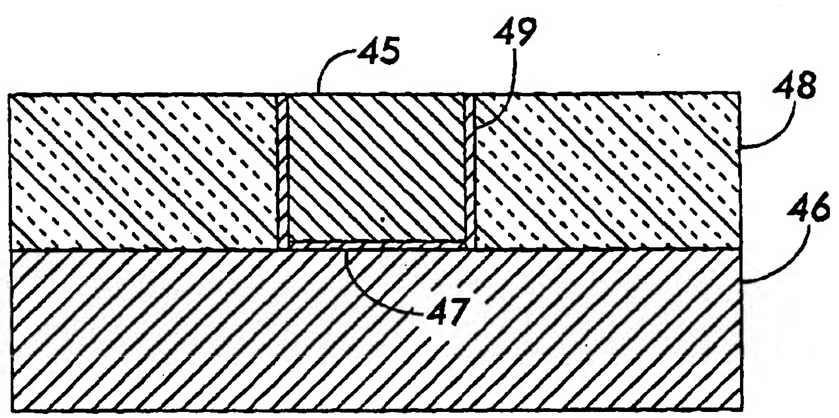
(74) Agent: BECHTEL, James, B.; NSWC-Dahlgren Division, Office of Patent Counsel, Code CD222, Building 183, Rm. 015, 17320 Dahlgren Road, Dahlgren, VA 22448-5100 (US).

(81) Designated States: CA, CN, IL, JP, KR, MX, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published

With international search report.

(54) Title: ELECTRONIC DEVICES WITH BARRIER FILM AND PROCESS FOR MAKING SAME



(57) Abstract

A semiconductor device having a barrier film (47) comprising an extremely thin film formed of one or more monolayers each comprised of a two-dimensional array of metal atoms. In one exemplary aspect, the barrier film (47, 49) is used for preventing the diffusion of atoms of another material (45) such as copper conductor, into a substrate (46), such as a semiconducting material or an insulating material, and an oxide layer (48). Methods for making the barrier film (47) in a semiconductor device are also covered. The extremely thin barrier film (47, 49) makes possible a significant increase in the component density and a corresponding reduction in the number of layers in large scale integrated circuits, as well as improved performance.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece			TR	Turkey
BG	Bulgaria	HU	Hungary	ML	Mali	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MN	Mongolia	UA	Ukraine
BR	Brazil	IL	Israel	MR	Mauritania	UG	Uganda
BY	Belarus	IS	Iceland	MW	Malawi	US	United States of America
CA	Canada	IT	Italy	MX	Mexico	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NE	Niger	VN	Viet Nam
CG	Congo	KE	Kenya	NL	Netherlands	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NO	Norway	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	NZ	New Zealand		
CM	Cameroon			PL	Poland		
CN	China	KR	Republic of Korea	PT	Portugal		
CU	Cuba	KZ	Kazakstan	RO	Romania		
CZ	Czech Republic	LC	Saint Lucia	RU	Russian Federation		
DE	Germany	LI	Liechtenstein	SD	Sudan		
DK	Denmark	LK	Sri Lanka	SE	Sweden		
EE	Estonia	LR	Liberia	SG	Singapore		

Description

Description

ELECTRONIC DEVICES WITH BARRIER FILM AND PROCESS FOR MAKING SAME

Statement of Government Interest

The invention described herein may be manufactured and used by or for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

Technical Field

This invention relates generally to the fabrication of electronic devices, and particularly to a novel barrier film for electronic and electro-optic materials.

Background Art

Integrated circuits (ICs) are composed of many millions (sometimes billions) of components such as transistors, resistors, and capacitors. These individual components are laid out in a two dimensional array on a substrate such as silicon or gallium arsenide. The two dimensional arrays are often stacked one on top of another to form a three dimensional IC. As in any circuit, these components, and the several layers, must be connected to one another electrically. Interconnection on the two dimensional surfaces is accomplished by depositing strips of metal that act as connecting "wires." Likewise, the layers are interconnected by metal plugs deposited in via holes made between layers. These steps in the manufacturing process are commonly referred

to as "metallization."

Generally, silicon is the substrate material of choice, aluminum is the metal of choice for two dimensional IC metallization, and tungsten is the metal of choice for filling via holes for multiple layer interconnection. Silicon is preferred because it is cheap and abundant. Aluminum and tungsten are chosen because they have adequate electrical conductivity and they can be made not to diffuse into the substrate during the many annealing operations inherent in the IC manufacturing process.

Because the electrical conductivity of aluminum and tungsten is limited, the "wires" and plugs must be made thick enough to ensure minimal resistance to electric current between components and between layers. The large size of these conductors has recently become an issue for IC designers and fabricators interested in placing a greater density of circuit elements on an IC. In order to achieve greater performance from ICs, the lateral dimensions of the circuit elements must be reduced. This reduction in IC element size has two detrimental effects on the resulting IC. First, it increases the resistance of the metal interconnects. Second, it increases the aspect ratio of the via holes, making them more difficult to fill with the metallic material. Incomplete filling of the via holes exacerbates the problem of high resistance. Today, there is often not enough space in the lateral direction on an IC chip to accommodate large aluminum conductors. Additionally, the size of the via holes, when

filled with tungsten, limits the number of levels in the IC to no more than five.

Copper, which is a much better conductor of electricity than aluminum, is available as an alternative metallization material. Because of copper's greater electrical conductivity, copper imposes less resistance to the flow of electrons than aluminum or tungsten conductors having equivalent dimensions. The increasing density of components on today's ICs requires the smaller sized conductors that are only achievable by the use of highly conductive metallization materials.

Unfortunately, copper has one notable problem. It has a tendency to diffuse into silicon at elevated temperatures. This has precluded copper as a metallization candidate because ICs must be annealed several times during the manufacturing process. In order for copper metallization to be feasible, a technique must be developed that will prevent the diffusion of copper into silicon. Among the possible solutions currently under development within the semiconductor industry the most prevalent is the use of nitrides of the transition metals titanium and tungsten. The thickness of the metal-nitride layer required to stop copper diffusion into silicon effectively is in the range of tens to hundreds of nanometers, or hundreds to thousands of Angstroms (Å).

The problem of diffusion exists not only in the case of copper metallization on silicon, but also in the case of copper metallization on other single- and polycrystalline

semiconductor substrate materials such as gallium arsenide, silicon carbide, germanium, and so forth. Copper diffusion into insulating materials such as SiO_2 can also result in short circuits, especially in dense arrays of IC components. Diffusion is also a problem with other high conductivity metallization materials such as gold, silver, and platinum.

An object of this invention is to provide a barrier film which is extremely thin, yet permits metallization using copper and other high conductivity metallic conductors which would otherwise have a tendency to diffuse into a substrate formed of a semiconducting or insulating material.

It is also an object of the invention to improve electronic and electro-optic devices by making it possible to achieve one or more of the following desirable characteristics: increased component density in large scale integration, reduced heat dissipation, increased speed of operation, and a decreased number of layers.

Still another object is to provide a procedure for forming an extremely thin diffusion barrier, which produces consistent results rapidly and reliably, and which is not highly dependent upon the accurate maintenance of operating conditions such as time and temperature.

Still another object is to provide a process for forming an extremely thin diffusion barrier which eliminates voids and mechanical stresses that can have detrimental effects on the substrate, the diffusion barrier, or the metallization layer.

Disclosure of the Invention

In accordance with this invention, a semiconductor device is fabricated by forming, on a surface of a substrate material, a barrier film having a monolayer of metal atoms immediately adjacent the surface of the substrate material. In one aspect, a metallic conductor, which has a tendency to diffuse into the substrate material, is then deposited onto the barrier film. Metallic conductors which have a tendency to diffuse into substrates of semiconductor or insulating materials include, for example, pure copper, copper alloys (e.g., Cu-Al, Cu-Si-Al), copper doped with a dopant (e.g., aluminum) that impedes electromigration, gold, silver, or platinum. For purposes of this invention, a "monolayer" is understood to refer to a two-dimensional array of atoms having the thickness of one atomic layer; although the monolayer may have minuscule defects such as minute portions with a thickness that exceeds one atomic layer and/or minute portions that are voids, the average thickness nonetheless essentially is an atomic layer providing essentially complete coverage of the directly underlying substrate surface regions. The monolayer, which is extremely thin by definition, serves as a barrier film, inhibiting diffusion of the metallic conductor into the substrate material. For purposes of this application, the material upon which the monolayer of atoms is formed is often generally referred to herein as a "substrate" for such formation, and it will be appreciated that the term "substrate" as used herein can encompass a bulk wafer or, alternatively, a layer that is

grown, deposited, formed or bonded upon another body. The present invention is especially concerned with substrates that are semiconductor or insulating materials.

In one preferred method of this invention, a monolayer is produced by depositing a metal halide upon a surface of a semiconducting or insulating substrate material where it first reacts with the substrate material and dissociates, releasing gaseous by-products formed of substrate atoms and halogen atoms of the precursor compound. This reaction is self-limiting resulting in formation of a monolayer of metal atoms on the substrate that thereafter enables a homoepitaxial film formed of the metal halide molecules to form thereon as the deposition process proceeds. This deposition operation can be carried out by various methods, but is preferably carried out by molecular beam epitaxy, or alternatively by r.f. sputtering. At this juncture, a temporary heteroepitaxial film has been formed on the substrate where the diffusion barrier is ultimately desired. Then, in a second stage of the procedure, the temporary heteroepitaxial film is subjected to a selective removal procedure, whereby the homoepitaxial portion of the deposited film having the halogen constituents is selectively eliminated while the monolayer of metal atoms remains behind attached to the surface of the substrate material. The removal procedure preferably is an annealing operation. Alternatively, chemical etching which is selective to remove the homoepitaxial portion of the deposited film while leaving the monolayer of metal atoms also can be used. In any event, the metal atom

monolayer strongly adheres to the substrate material, and is not adversely affected by extended annealing times, high annealing temperatures, or chemical etching conditions.

The precursor compound preferably comprises a metal halide, e.g., a barium, strontium, cesium or rubidium- halide salt. The thickness of the monolayer basically corresponds to the diameter of the metal atom constituent(s) of the monolayer. Metal atoms of barium, strontium, cesium, rubidium, and so forth have a thickness (i.e., the diameter of the largest electron orbital) of less than 5 Å, so it can be appreciated that an extremely thin diffusion barrier layer is achieved by this invention. The semiconducting substrate materials that can be processed according to this invention include mono- or polycrystalline, doped or undoped, semiconductors, such as silicon, germanium, indium phosphide, gallium arsenide, silicon carbide, gallium nitride, aluminum nitride, indium antinomide, lead telluride, cadmium telluride, mercury-cadmium telluride, lead selenide, lead sulfide, tertiary combinations of these materials, and so forth. The insulating substrate materials that can be processed according to this invention include doped or undoped silicon oxides (e.g., silicon dioxide), silicon nitride, phosphosilicate glass (PSG), borophosphosilicate glass (BPSG), barium fluoride, strontium fluoride, calcium fluoride, and so forth.

In a further embodiment of this invention, a multiplicity of monolayers are formed contiguous with each other upon the substrate surface. This embodiment can become advantageous such

as where a substrate is involved having a relatively greater surface roughness and it is necessary to account for any discontinuities in the surface profile by sufficiently building-up the diffusion layer to blanket the surface topography presented and provide complete coverage. To build-up multiple monolayers, one stacked upon the other, MBE deposition can be used to sequentially deposit additional monolayers of metal atoms using an elemental source of the metal. In this way, a diffusion barrier film thickness can be assembled up to any desired thickness, but preferably is maintained at or below not more than 100 Å, more preferably not more than 20 Å to meet the primary objective of providing an extremely thin yet effective diffusion barrier.

As can be appreciated, a semiconductor device is obtained by this invention in which a monolayer or several monolayers of metal atoms separates a metallic conductor from other materials in the device, such as semiconductor or insulating materials, in which the extremely thin diffusion barrier film serves as an effective barrier preventing atoms of the metallic conductor from diffusing into such other materials and either impairing the device or rendering it totally inoperative.

Various other objects, details and advantages of the invention will be apparent from the following detailed description when read in conjunction with the drawings.

Brief Description of Drawings

FIG. 1 is a schematic cross-section depicting diffusion of copper into a silicon substrate, where no diffusion barrier is present;

FIG. 2 is a graph illustrating the projected requirement in diffusion barrier thickness by the Semiconductor Industry Association;

FIG. 3 is a schematic cross-section depicting the effect of a diffusion barrier in accordance with the invention;

FIG. 4 is a schematic diagram illustrating the process of deposition of a diffusion barrier precursor compound, and a metallization layer, onto a substrate by molecular beam epitaxy;

FIGS. 5A-E is a schematical illustration showing the interfacial structure of the diffusion barrier on an atomic level as it is being formed on a semiconductor substrate after various process steps according to an inventive process;

FIG. 6 is a schematic diagram illustrating the process of deposition of a diffusion barrier precursor compound onto a substrate by r.f. sputtering; and

FIG. 7A is a schematical illustration showing the interfacial structure of the barrier film on an atomic level where the barrier film is comprised of a plurality of contiguous monolayers, while FIG. 7B shows another embodiment of the invention where the barrier film is a composite monolayer formed of different types of metal atoms, and FIG. 7C shows yet another embodiment where the barrier film is

comprised of a plurality of contiguous monolayers in which different monolayers thereof are formed of different types of metal atoms.

FIG. 8 is a schematic cross-sectional view showing a diffusion barrier in accordance with the invention preventing diffusion of a copper plug into silicon substrate and into a silicon dioxide insulating layer overlying the substrate.

Best Mode for Carrying Out the Invention

FIG. 1 illustrates a typical attempt at copper metallization of a silicon semiconductor substrate 10. The substrate, which is made up of silicon atoms 12, has two laterally delineated copper interconnect strips 14 deposited on its surface. In the annealing process, copper atoms 16 tend to diffuse into the substrate, impairing its semiconducting properties, and usually rendering it totally inoperative, by effectively creating an electrical short circuit. Similar diffusion occurs at an interface between a copper conductor and a SiO_2 insulating layer, for example in the case in which an attempt is made to deposit a conducting copper plug in a via hole in the SiO_2 insulating layer. Diffusion of copper atoms into the SiO_2 insulating layer impairs its effectiveness as an insulator and may have a serious adverse effect on the properties of the device.

As mentioned above, various attempts have been made to achieve a diffusion barrier to permit the use of copper conductors in semiconductor devices. The most attention so far

has been given to the use of nitrides of tungsten and titanium. Various other diffusion barrier materials, for example tantalum nitride, have also been tried. As shown in FIG. 2, which is based on published Semiconductor Industry Association data, presently achievable diffusion barrier thicknesses are only in the 200-250 Å range for tantalum nitride, although thicknesses smaller than that are expected to be pursued by the industry in the upcoming years.

This invention provides an effective diffusion barrier having a thickness well below 100 Å, and below 5 Å in one exemplary embodiment, which is far below the minimum thickness projected by the industry data depicted in FIG. 2. The extremely thin diffusion barrier layers achievable by this invention potentially could be useable long after alternative technologies become obsolete.

Referring now to FIG. 3, a portion of an integrated circuit is schematically illustrated on an atomic level that comprises a silicon substrate 18 made up of silicon atoms 20, and having laterally delineated copper interconnect strips 22. At the upper surface of the silicon substrate 18, a monolayer of barium (Ba) atoms 24 is interposed between the conductor strips 22 and the surface of the substrate 18 and effectively prevents diffusion of the copper atoms into the silicon. The layer of Ba atoms need only have a thickness of one atomic layer, i.e., a monolayer of approximately 5×10^{-10} meters (5Å) in thickness, in order to provide the desired barrier to diffusion of the conductor into the adjoining substrate. The

barium layer depicted in Fig. 3 illustrates the situation in which a single monolayer of barium is provided. The extremely small thickness of the diffusion barrier contributes to the reduction in both thickness and the lateral dimensions of the integrated circuit layer, and the ability to use copper interconnects and other conductor materials otherwise predisposed to creating diffusion problems (e.g., Au, Ag, Pt) instead of aluminum interconnects. As such, the present invention represents a remarkable breakthrough in the field.

As will become apparent from the following description, in one mode of this invention, a diffusion barrier comprised of metal atoms and having a thickness of not more than approximately 5Å is achievable by depositing a metal halide precursor compound on a semiconductor or insulating substrate so as to form a temporary heteroepitaxial film thereon. Then, the resulting temporary heteroepitaxial film created by the metal halide and the substrate surface is subjected to a post-growth anneal or chemical etching in which all of the temporary heteroepitaxial film is eliminated by removal from the substrate except for an atomic layer of the metal component, i.e., a monolayer. This residual monolayer of metal atoms disposed in contact with the substrate surface provides a diffusion barrier to conductor materials.

One suitable approach for depositing the metal halide used as a precursor compound for forming the diffusion barrier layer is molecular beam epitaxy (MBE), such as depicted in FIG. 4. A substrate 26, e.g., a silicon wafer, is supported on a rotating

holder 28 within a conventional MBE deposition chamber 30. The deposition chamber is illustrated in simplified form. Not shown are provisions for raising the temperature of the substrate to annealing temperatures and for evacuating the chamber. Also not shown is a conventional Reflective High Energy Electron Diffraction (RHEED) diagnostic system directed toward the substrate 26.

A diffusion barrier precursor compound effusion cell, for example a barium fluoride, strontium fluoride or the like effusion cell, is provided at 32, and has a shutter 33. A shutter 35 is also provided for the silicon wafer 26. An electron beam source for the metallization layer, e.g., copper, is shown at 34.

In the operation of the MBE deposition apparatus of FIG. 4, the substrate 26 is placed inside the chamber 30 and positioned by rotatable holder 28 and the chamber 30 is evacuated, using ion pumps and liquid nitrogen trapping to achieve a high vacuum. The substrate 26 is vacuum annealed to remove any passivation layer by deoxidation, for example silicon dioxide in the case of a silicon wafer.

The temperature of the substrate 26 is then reduced to a suitable deposition temperature, and the effusion cell 32 is heated while the substrate 26 is mechanically rotated. The electron beam of a RHEED diagnostic system is focused onto the substrate 26 and the RHEED pattern is monitored. When the RHEED pattern corresponding to the single crystal substrate surface appears (indicating complete removal of the passivation

layer) on the RHEED screen, the shutters 35 and 33 in front of the substrate holder 28 and the effusion cell 32, respectively, are opened to allow precursor molecules to impinge on the substrate surface 29. Deposition of the precursor 27 onto the silicon surface 29 begins, and is allowed to continue until the single crystal silicon RHEED pattern disappears and is replaced by a pattern corresponding to a single crystal layer of the precursor compound. Deposition is halted by closing the substrate and effusion source shutters 35 and 33, respectively. By this juncture, a temporary heteroepitaxial film derived from the precursor molecules is situated on the substrate surface 29, although the nature of the interface is more complicated as will become apparent from later descriptions herein.

During the deposition of the precursor 27 on the substrate 26, the substrate 26 should be at a temperature in the range from approximately 500°C to 800°C, and ideally at approximately 750°C, though the temperature will vary depending on the particular substrate and the processing tool. The pressure within the deposition chamber 30 should be 10^{-8} mbar or less, more preferably 10^{-9} mbar or less, and still more preferably 10^{-10} mbar or less, in the case of depositing a metal halide on a silicon substrate. The time required to achieve adequate deposition of the precursor sufficient to form the temporary heteroepitaxial film on the substrate is typically one or two minutes, but is not limited thereto.

Following the deposition on the substrate of the temporary heteroepitaxial film derived from the precursor compound, the

temperature of the substrate is raised to cause precursor molecules to detach from the temporary heteroepitaxial film on the substrate. In the case of BaF_2, barium atoms adjacent to the substrate remain tightly adhered thereto as a two-dimensional monolayer, while fluorine atoms (as bonded to other barium atoms) in the temporary heteroepitaxial film are effectively re-evaporated in the form of barium fluoride and eliminated from the temporary heteroepitaxial film. This will cause the RHEED pattern to change in appearance. Specifically, the "reappearance" of a RHEED pattern similar to that for the single crystal substrate confirms that the precursor molecules have been evaporated. The substrate temperature at which the detachment of the precursor molecules with the halogen atoms from the temporary heteroepitaxial film takes place during the post-growth anneal step is not necessarily limited, but should be in the vicinity of 750°C to 1000°C, preferably 800°C. The monolayer of metal atoms which remains on the substrate serves as the diffusion barrier between the substrate and any metallization layer subsequently deposited upon it. The metallization layer can be deposited by any of various standard microelectronic metallization methods, and, in this embodiment, it can be conveniently deposited while the substrate is still in the MBE chamber by operation of the electron beam source.

The crystallographic and chemical characterization of the aforesaid temporary heteroepitaxial film, and the effect of treatments thereof according to this invention to form a diffusion barrier film on the substrate, are now discussed in

greater detail. Based on X-ray photoelectron spectroscopy (XPS) and heavy ion backscattering spectroscopy (HIBS) analyses of the precursor compound/substrate surface interfacial chemistry, the formation of an ultra-thin metal monoatomic layer (monolayer) on the substrate is considered to proceed by a multi-stage process, which is schematically illustrated in FIGs. 5A-E. XPS and HIBS analysis measurements referred to herein can be performed using generally available equipment and analyses protocol understood and implementable by one skilled in the art.

As schematically illustrated in FIG. 5A, BaF_2 molecules 50 are directed and impinged onto the surface 51 of a silicon substrate 52, such as by MBE deposition. For FIGs. 5A-E, BaF_2 is used to illustrate the metal halide, and silicon is used to illustrate the (semiconductor) substrate, although other materials can be used as indicated elsewhere herein.

Ideally, the silicon surface 51 to be used as the deposition substrate has a highly planar, smooth surface to minimize the coating thickness needed to provide complete coverage thereof. Deoxidation annealing, chemical-mechanical-planarization (CMP) polishing or ion milling can be used in a pretreatment of the silicon surface prior to deposition of the diffusion barrier to enhance the planarity and smoothness of silicon surface, if necessary. On the other hand, as will be described below, the inventive process itself provides some measure of *in situ* planarization of the silicon surface during MBE deposition.

In any event, in the first step, the BaF_2 molecules react with silicon atoms 51a, 51b, 51c, and so forth, at the surface 51 of the silicon substrate 52. The Ba-F and silicon-silicon bonds at the surface of the silicon substrate are broken. As schematically shown in FIG. 5B, the free silicon and fluorine atoms at the vicinity of the interface where the barium fluoride molecules are contacting the silicon surface 51 then combine to form volatile silicon-fluoride compounds (SiF_y) 53 which escapes from the silicon substrate surface 51, and it is extracted from the MBE chamber via vacuum. Although FIG. 5B depicts compound 53 as two halide atoms (white circles) bonded to a common metal atom (darkened circle), it will be understood that this illustrative only because other gaseous metal-halides may be generated, such as tetrahalides of silicon where the substrate 52 is silicon. By comparison, if the substrate 52 instead is GaAs, the escaping gas 53 would be GaF. This etching-like effect upon the surface silicon atoms serves to effectively smoothen the silicon surface. In any event, as illustrated in FIG. 5B, the barium atoms left behind bond with dangling bonds of the surface silicon atoms, forming a monoatomic layer 54 of metal atoms, i.e., a metal monolayer of barium atoms. This deposition step proceeds for a sufficient duration of time to form a continuous layer of barium atoms across the surface of the silicon substrate without leaving any bare spots.

As illustrated in FIG. 5C, once complete coverage of the silicon substrate 52 with barium atoms 54 is achieved, barium

fluoride 50 deposition via MBE is continued from a molecular beam. As illustrated in FIG. 5D, this subsequently introduced barium fluoride adheres to the barium monolayer 54 and grows epitaxially thereon to form a temporary homoepitaxial film portion 55. The amount of subsequent deposition of epitaxial barium fluoride on the barium monolayer is allowed to be enough to provide a safety measure which ensures complete substrate coverage with a monolayer of barium atoms. In this way a heteroepitaxial film 56 is formed on the substrate surface 51 comprising a monolayer 54 of metal (e.g., Ba) atoms as an interaction regime attached directly to the substrate surface 51 and a homoepitaxial regime 55 comprised of oriented molecular metal halide (e.g., barium fluoride) formed, in turn, on the monolayer 54. The homoepitaxial regime 55 of BaF_2 of the temporary heteroepitaxial film 56 is (100)-oriented on silicon (100), and (111)-oriented when the substrate is silicon (111), GaAs (100), or GaAs (111).

XPS measurements have confirmed that barium atoms have the two above-mentioned different chemical states, i.e., the interaction (metal monolayer) and the homoepitaxial regimes, in the temporary film present at this stage of processing. The relative abundance of these two states has also been determined by XPS. The number of barium atoms in each state is determinable by normalizing integrated XPS peak intensities to HIBS measurements of the total number of barium atoms on the surface. The results of these analyses confirm that BaF_2 first reacts with the silicon surface during initial MBE deposition

at the silicon surface and dissociates, releasing a gaseous silicon-fluorine compound. This reaction is self-limiting, resulting in a barium monolayer that enables subsequent BaF_2 molecules to form an epitaxial (111)-oriented film on the silicon surface. Then, a post-growth anneal affects evaporation of the barium fluoride deposited on the monolayer.

That is, as illustrated in FIG. 5E, in a second stage of this inventive procedure, which is conducted after the MBE deposition of the metal halides on a substrate to form the temporary heteroepitaxial film 56 shown in FIG. 5D, a vacuum anneal is performed to cause evaporation of barium fluoride 57 from the temporary heteroepitaxial film such that the barium fluoride content found in the homoepitaxial portion thereof (feature 55 in FIG. 5D) is completely removed back to the monolayer 54 of barium atoms attached to the silicon surface 51. Alternatively, the homoepitaxial portion 55 of the temporary heteroepitaxial film can be removed by etching (e.g., chemical etching) which is selective between the homoepitaxial portion 55 and the monolayer portion 54 such that the former can be removed while leaving the latter intact.

In any event, prior to performing the post-growth anneal (or etching) to remove the homoepitaxial portion 55 of the temporary heteroepitaxial film, there is no practical limit on how thick the overdeposit of barium fluoride can be that is formed over the barium monolayer. However, it will be appreciated that the thicker the deposited barium fluoride layer(s) of the homoepitaxial portion of the temporary film is

made to be, the longer the post-growth anneal time that will be necessary to decompose the deposited thickness of barium fluoride molecules back to the monolayer of barium atoms left attached to the substrate surface.

The MBE deposition of the temporary heteroepitaxial film and the post-growth anneal can be performed in the same processing chamber without breaking the vacuum between the two procedures. Alternatively, the MBE deposition can be performed in a first processing tool, after which the vacuum is broken, and the workpiece is then transferred to another processing tool for separately performing the post-growth anneal at which time the substrate is heated up again with a vacuum being created in the second processing tool. In the latter case, the homoepitaxial portion of the temporary heteroepitaxial film serves as a protective coating over the monolayer portion of the heteroepitaxial film during such transit between separate processing tools.

In that the atomic diameter of barium is 4.48 Å, and that of strontium is 4.29 Å, it can be appreciated how the formation of a monolayer of these metal atoms, for example, on a substrate by the techniques presented herein permits the formation of an extremely thin, yet effective diffusion barrier.

While not desiring to be bound to any particular theory, it nonetheless is thought that the underlying mechanism by which the metal monolayer prevents diffusion of the copper, or other highly diffusive metal, through the barrier layer into

the semiconductor or insulating substrate is at least in part attributable to the fact that metal atoms are provided in the monolayer which have relatively large electron clouds which can overlap or touch each other between the metal atoms to effectively form an energy barrier against movement of copper atoms therethrough. As will be understood by one of ordinary skill in the art, from a standpoint of terminology, the electron clouds are also spoken of as atomic orbitals occupied by electrons in different energy levels or shells, and the electron cloud is a cloud of negative charge formed of electrons of an electron density distribution corresponding to the element at issue.

An important advantage of the invention is the ease with which the diffusion barrier layer can be formed. Where metal halides are used as a precursor in forming the diffusion barrier film, the precursor, e.g., BaF_2 or SrF_2, can be deposited for a sufficient duration of time to ensure complete coverage of the silicon substrate. Such complete coverage can be achieved within relatively short period of time, e.g., about one minute using MBE deposition of a metal halide on the substrate, depending on deposition conditions. Also, the length of deposition time is not critical provided it is at least high enough to establish the diffusion barrier film; deposition times of several minutes are not detrimental to the procedure, and the deposition temperature also is not critical. In the second step, all components of the precursor except for the monolayer of metal atoms, are removed by the post-growth

annealing procedure. The metal atoms of this thin layer adhere tightly to the substrate, and consequently, the second step can be carried out over a wide range of time and temperature conditions without adversely affecting the formation and character of the diffusion barrier layer.

By way of a specific illustration of forming a diffusion barrier on a semiconductor substrate, BaF_2 can be used as the barrier film precursor and a silicon wafer can be used as the substrate. The silicon substrate first is deoxidized by vacuum annealing at 900°C for one hour to remove the silicon dioxide passivation layer. Then the substrate can be brought to a deposition temperature of 750°C in a VG Semicon V80H MBE growth chamber at a vacuum of less than 1×10^{-10} mbar. All temperature measurements are made from a noncontact thermocouple gauge. A BaF_2 effusion cell can be heated to 1050°C. While the substrate holder is mechanically rotated, an electron beam from a RHEED diagnostic system is directed toward the substrate. The beam is focused until the RHEED pattern of a single crystal silicon surface appears on the RHEED screen. The shutters in front of the substrate holder and the effusion cell are then opened to allow BaF_2 molecules to impinge on the substrate surface. Deposition of BaF_2 is allowed to continue until the single crystal silicon RHEED pattern disappeared and is replaced by a single crystal BaF_2 pattern. Deposition is then halted by closing the substrate and effusion source shutters. The substrate temperature is then raised to 800°C and held until a RHEED pattern similar to that of the single crystal

silicon substrate reappears. It will be understood that the above-provided exemplary protocol is provided merely for sake of illustration, and not limitation.

In the mode of the invention being discussed above in which metal halides are used as precursor compound for forming the diffusion barrier film, the precursor compounds that can be used include, for example, BaF_2, $BaCl_2$, SrF_2, $SrCl_2$, CsFl, CsCl, RbF, and RbCl, and the like. Especially preferred are those metal halide salts that have cubic halide, e.g. a cubic fluorite, crystal structure. While not desiring to be limited to any particular theory at this point, applicants nonetheless consider that precursor compounds obtainable as metal halides, e.g., BaF_2, $BaCl_2$, SrF_2, $SrCl_2$, CsFl, CsCl, RbF, and RbCl, and the like, that have cubic crystal structure will tend to provide sources of metal atoms that are amenable to the above-discussed decomposition reaction and interaction with the silicon surface under readily implementable MBE and annealing processing conditions. Although not desiring to categorically exclude all metal halide salts having rutile crystal structure, rutile metal halide salts may not be suitable for many processing environments as they do not normally decompose under typical MBE conditions.

In another mode of the invention for forming the diffusion barrier film, the monolayer of metal atoms alternatively can be formed in a one step operation (i.e., without a post-growth anneal step) by directly depositing an elemental form of the metal atoms, such as barium, via MBE on the surface of the

semiconductor substrate. Since certain elemental metals such as barium are highly reactive, appropriate precautions have to be taken to handle, maintain and process the elemental barium in an inert environment, e.g., under an argon gas atmosphere, up until it is deposited upon the semiconductor.

Also, in another embodiment of this invention, it is possible to form the monolayer of metal atoms directly on the semiconductor substrate by the above-described two-step decomposition reaction process involving a metal halide (i.e., MBE deposit/post-growth anneal), and then to increase the thickness of the diffusion barrier film by depositing one or more additional monolayers of metal atoms on the original monolayer through depositing the elemental form of the metal atoms, such as barium, via MBE on the original monolayer. That is, while formation of a single monolayer on the substrate as described above is sufficient to meet the diffusion barrier objectives of this invention, it is also within the scope of this invention to form one or more additional monolayers of the metal on the original monolayer as long as the overarching objective of forming a diffusion layer of extremely small thickness is maintained. For example, the metal atom can be deposited from an elemental form via MBE on the surface of the silicon substrate. In this way, a plurality of monolayers can be formed as contiguous layers upon the substrate to form an overall thickness in the diffusion barrier layer of any desired thickness. Since thin thicknesses are desired, the diffusion barrier preferably is built up to an overall thickness that

does not exceed 100Å, and more preferably does not exceed 20Å. FIG. 7A illustrates this scenario in which a plurality of monolayers 71a, 71b, and 71c are sequentially formed, upon the surface 72 of substrate 73, one on the other, in the manners described above. Then, a conductor material or other material (not shown) can be formed over the outermost monolayer 71c. In this embodiment, each of monolayers 71a, 71b, and 71c are formed of the same type of metal atoms, and together, they form the barrier film. Also, while three monolayers are depicted in FIG. 7A, the plurality of monolayers can be two or more.

Also, it is possible to deposit a combination of different types of metal atoms during precursor deposition on a substrate to form a composite diffusion barrier monolayer. For example, because the melting and sublimation temperatures of strontium fluoride and barium fluoride are similar, the temperature ranges for MBE deposition of a strontium fluoride precursor onto silicon and for the evaporation of the strontium fluoride precursor from silicon almost completely overlap those given above for barium fluoride. Thus, temperatures in the mid-portion of the ranges given for barium fluoride on silicon are also satisfactory for the MBE deposition and evaporation of strontium fluoride. However, the temperatures required to sublimate, i.e., directly change the state of the source solid crystal form to a gas for deposition via MBE, for barium fluoride and strontium fluoride are slightly different. Consequently, to control the ratio of barium to strontium in a composite monolayer of a barrier layer to be formed, the barium

fluoride and strontium fluoride should be deposited using separate effusion cells for the MBE chamber. In any event, a composite monolayer can be formed of barium and strontium atoms in this manner. FIG. 7B illustrates this embodiment of the invention where the barrier film is a composite monolayer 71 formed of different types of metal atoms 71d and 71e. Two or more different types of metal atoms can be provided in the composite monolayer 71. Then, a conductor material or other material (not shown) can be formed over the composite monolayer 71.

Also, if an additional monolayer or monolayers are deposited on the original monolayer formed on the surface of the substrate, the different monolayers can have the same or different types of metal atoms by appropriate selection of the precursor compounds at the different stages of processing. For instance, as illustrated in FIG. 7C, the barrier film is comprised of a plurality of contiguous monolayers 71f, 71g and 71h in which different monolayers thereof are formed of different types of metal atoms. In this illustration, layers 71f and 71h are formed of the same type of metal atoms while intervening monolayer 71g is formed of a metal atom that is different from the metal atoms in layers 71g and 71h. However, there is no requirement that barrier film arrangements with three or more monolayers containing the different types of metal atoms must alternate through the stack of monolayers in any particular pattern. Also, while three monolayers are depicted in FIG. 7C, the embodiment is not limited to that

plural number. Also, composite monolayers, such as described in FIG. 7B can be used in combination with one or more contiguous monolayers formed thereon having a single type of metal atoms, such as shown in FIG. 7A, or different types of metal atoms in different respective monolayers, such as illustrated in FIG. 7C.

As yet another mode of applying the metal halide precursor to the substrate to form the temporary heteroepitaxial film, r.f. sputtering, such as depicted in FIG. 6, can be used. In a sputtering chamber 36, an argon-ion gun 38 directs a beam 40 onto a supply (target) 42 of barium fluoride, for example, causing deposition of barium fluoride onto a substrate 44 by sputtering. Here, as in the case of MBE deposition, the post-growth annealing of the substrate can take place within the sputtering chamber in order to remove BaF_2 molecules and the fluorine atoms leaving only a thin layer of barium atoms as a monolayer adhering to the surface of the substrate. The metallization (conductor) layer can also be applied to the substrate while it is inside the sputtering chamber. Sputtering can also be used to deposit a diffusion barrier of other metal atoms, such as strontium atoms, in a similar manner. Also, a combination of different types of metal atoms could be sputtered in the same monolayer or in different monolayers using different sputtering targets formed of different respective metal halide precursors. In general, however, MBE is superior to r.f. sputtering because sputtering can cause dissociation of the barium-fluorine bond before the

barium fluoride molecule reaches the substrate surface which facilitates the formation of the temporary heteroepitaxial film.

As other different modes for forming the diffusion barrier film on a substrate, deposition processes other than MBE and r.f. sputtering can be used, for example, physical and chemical vapor deposition, wet chemical processes, and liquid phase epitaxy. For instance, precursors used in metal-organic chemical vapor deposition (MOCVD) to form the diffusion barrier on a semiconductor or insulating substrate include Ba (2,2,6,6-tetramethyl-3,5 heptanedionate) and Sr (2,4-pentanedionate).

As illustrated in FIG. 8, the diffusion barrier produced in accordance with the invention can be used not only to prevent diffusion of conductor metals into a semiconductor substrate, but also to prevent diffusion of the conductor metal into an insulating layer. In FIG. 8, layer 46 is a semiconductor substrate, for example, a semiconducting layer of silicon, and layer 48, which overlies layer 46, is an insulating layer of silicon dioxide (SiO_2). A plug 45 of a metal, such as copper, is located in a via hole though insulating layer 48, and makes ohmic contact with the semiconducting layer 46 through a thin diffusion barrier layer 47 of barium formed by one of the processes described above. This plug is used to conduct current between layer 46 and another layer (not shown) which is separated from layer 46 by insulating layer 48. In the same process, the sidewall of the via hole is lined with a barium diffusion barrier 49, which

prevents diffusion of the copper into the insulating layer. The barium or strontium atoms are deposited onto an insulating layer in the same way in which they are deposited onto silicon.

As will be apparent from FIG. 8, the minimization of the thickness of the side wall diffusion barrier 49 makes it possible to use copper for interconnections between layers. The copper interconnects can be significantly narrower than tungsten interconnects having the same current capacity, and the diffusion barrier is also very thin. Therefore the use of the diffusion barrier in accordance with the invention as a liner for via holes in insulating layers, can contribute significantly to the minimization of the lateral dimensions of an integrated circuit of which the elements shown in FIG. 8 are a part. Because the diffusion barrier 49 is very thin, it permits the use of via holes of relatively low aspect ratio, making them easier to fill with conducting metal and eliminating voids which result in failures or rejection of ICs.

It will be understood that this invention is not limited to the above-illustrated substrate materials, conductor materials, and materials used to make the diffusion barrier, as long as other criterion understood and set forth herein for these respective materials are satisfied.

For instance, the material used for forming the diffusion barrier can be any appropriate metal in elemental form or precursor molecular compound from which a layer of metal atoms (i.e., a monolayer) can be formed on a semiconductor or insulating substrate.

The substrate material upon which the diffusion barrier is formed is not particularly limited and can include semiconductor materials and insulating materials used in semiconductor device fabrications. The semiconductor material can be, for example, Si, Ge, InP, GaAs, SiC, GaN, AlN, InSb, PbTe, CdTe, HgTe, $Hg_zCd_{1-z}Te$, PbSe, PbS, and tertiary combinations of these materials. The semiconductor material can be monocrystalline or polycrystalline. The semiconductor substrate can be in bulk wafer form, deposited or grown layer form (e.g., epitaxially grown), or silicon-on-insulator (SOI) form. The semiconductor can be doped or undoped with impurities (e.g., p-, n-doping). The insulating substrate material can be, for example, SiO_x, SiO_2, BaF_2, SrF_2, CaF_2, silicon nitride, PSG, or BPSG. For example, a thin diffusion barrier film formed of a barium, strontium or cesium monolayer (or monolayers) can be used to line via holes in insulators made of BaF_2, SrF_2 and CaF_2.

As to the types of conductor materials that can be formed on the diffusion barrier, these include conventional metals and metal alloys used for wiring line, interconnects, bonding pads, and so forth, in semiconductor device or opto-electronic device fabrication. The present invention is especially useful for providing an *in situ* barrier to electrically conductive metals which tend to diffuse into semiconductor and insulating materials common to semiconductor processing. These conductive metals include, for example, pure copper, copper alloys (e.g., Cu-Al, Cu-Si-Al), copper doped with a dopant (e.g., aluminum)

that impedes electromigration, gold, silver, or platinum. In the case of copper, it may be desirable to alloy it with small percentages (e.g., < 5%) of other metallic substances to prevent electromigration. The conductor material can be deposited on the diffusion barrier by any conventional technique, including, e.g., electroplating, electroless deposition, sputtering, chemical vapor deposition, e-beam evaporation, and so forth. For example, copper can be deposited by e-beam evaporation at 1×10^{-9} millibars in a heated chamber, or at 10×10^{-11} millibars under a nitrogen environment. The conductor film can be patterned on the diffusion barrier by various techniques, such as by conventional additive or subtractive processes known and used in semiconductor processing (e.g., photolithographic processing). The invention can also be used to prevent diffusion of gallium and/or arsenic from gallium arsenide into silicon and other substrates.

A number of advantages and improvements are achieved by the present invention which can be exploited in the semiconductor device processing industry. A principal advantage of this invention is that the thickness of the diffusion barrier layer can be made extremely thin. In practice, depending on the surface characteristics of the substrate material onto which the diffusion barrier layer is deposited, the thickness of the diffusion barrier layer according to this invention will generally be formed in the range of approximately 5 Å to 100 Å. In the case of a smooth, highly planarized substrate material, e.g., a substrate having a

surface roughness well below 5Å, the diffusion barrier can be made as thin as one monolayer, which will have a thickness slightly less than 5 Å corresponding the atomic diameter of the metal atoms forming the diffusion barrier. For such smooth substrates, the diffusion barrier formed of one monolayer having a thickness less than 5Å in thickness will satisfactorily inhibit diffusion of copper and other conductors into the substrate. With substrate materials having a relatively greater surface roughness, the thickness of the diffusion barrier layer will tend to vary. For instance, the diffusion barrier layer on a substrate having a surface roughness greater than 5Å may be formed so as to have a thickness value in the range of approximately 5 to 100 Å, with metal atoms of the diffusion barrier layer accumulating at any step edges on the substrate surface. Thus, the diffusion barrier film of this invention is only one monolayer or a multiple number of contiguous monolayers formed on the substrate surface, and in any event, it need not be more than approximately 100Å in total thickness to achieve the objectives of this invention for current and future anticipated semiconductor device fabrication specifications. A large scale integrated circuit having copper conductors and a diffusion barrier film according to this invention with a thickness in the range of approximately 5Å to approximately 100Å, can achieve an extremely high component density, which reduces the number of layers required for a given number of components, and very low heat dissipation. In the practice of this invention,

therefore, the diffusion barrier thickness can vary from a thickness less than about 5Å to a greater thickness, which can be up to about 100Å, preferably up to no more than 20Å. Conventional alternative diffusion barriers are significantly thicker than 100Å.

Another advantage of the invention is that the diffusion barrier film, where it is barium or strontium, or a similar metal, is compliant, i.e., it is mechanically soft and easily deformable. The compliance of the diffusion barrier film allows dissimilar materials to be put together without introducing defects, such as voids or mechanical stresses, at the interface which may have detrimental effects on device performance, the diffusion barrier film, or the metallization layer. Furthermore, barium and strontium, or like metals, can form intermetallic compounds with copper ($BaCu_{12}$ and Cu_5Sr are examples), causing copper atoms to be tightly bound to the barium or strontium at the interface and unable to migrate past the barium or strontium layer into the silicon.

Also, while the barrier film based on one or more monolayers of metal atoms that is used in this invention has been illustrated herein specifically as a barrier to diffusion of metal conductors into substrate materials, it will be understood that the barrier film is not necessarily limited to that use alone, as it possesses many advantageous attributes that could be exploited in semiconductor device fabrications. For example, the barrier film could be used as a barrier layer in the fabrication of semiconductor laser devices, such as

those having heterojunctions and incorporating different semiconductor materials, e.g., GaAs on top of silicon.

While the invention has been shown and described with reference to certain preferred embodiments, it will be understood by those skilled in the art that changes in form and detail may be made without departing from the spirit and scope of the appended claims.

Claims

Claims

1. A semiconductor device, comprising:

a substrate (18), a barrier film (24) on the substrate (18), a material (22) directly on the barrier film (24);

characterized in that the barrier film (24) includes a monolayer on the substrate (18).

2. A semiconductor device according to claim 1, wherein the barrier film (24) has a thickness less than 100Å.

3. A semiconductor device according to claim 1, wherein the barrier film (24) has a thickness less than 20Å.

4. A semiconductor device according to claim 1, wherein the monolayer of the barium film (24) comprises metal atoms selected from barium atoms, strontium atoms, cesium atoms, and rubidium atoms, singly or in combinations thereof, located on said surface of said substrate (18).

5. A semiconductor device according to claim 1, wherein the barrier film (24) comprises a plurality contiguous monolayers (71a-c) of metal atoms located on the surface of the substrate material (18).

6. A semiconductor device according to claim 1, wherein the barrier film (24) comprises a plurality of contiguous monolayers comprising two or more different types of metal

atoms selected from the group consisting of barium atoms, strontium atoms, cesium atoms, and rubidium atoms, located on said surface of said substrate (18).

7. A semiconductor device comprising:

a substrate (18) having a surface, a barrier film (24) on the substrate (18), a material (22) directly on the barrier film (24);

and characterized in that the barrier film (24) is comprised of a layer of elemental metal atoms attached to said surface.

8. A semiconductor device comprising:

a substrate (18), a barrier film (24) on the substrate (18), a material (22) directly on the barrier film (24);

and characterized in that the barrier film (24) has a thickness less than 100Å.

9. A semiconductor device comprising:

a substrate material (18) having a surface, a barrier film (24) on the substrate surface, a conductor (22) directly on the barrier film (24), and the conductor (22) having a tendency to diffuse into the substrate material (18) if in direct contact therewith;

characterized in that the barrier film (24) has a layer comprising elemental metal atoms attached to the substrate surface surface, and wherein the barrier film layer (24)

comprising elemental metal atoms serves as a barrier, inhibiting diffusion of the conductor (22) into the substrate material (18).

10. A semiconductor device according to claim 9, wherein the barrier film (24) has a thickness of not more than approximately 100Å.

11. A semiconductor device according to claim 9, wherein the barrier film (24) has a thickness of not more than approximately 20Å.

12. A semiconductor device according to claim 9, wherein the barrier film (24) has a thickness of not more than approximately 5Å.

13. A semiconductor device according to claim 9, wherein the monolayer of the barium film (24) comprises metal atoms selected from barium atoms, strontium atoms, cesium atoms, and rubidium atoms, singly or in combinations thereof, located on said surface of the substrate (18).

14. A semiconductor device according to claim 9, wherein the barrier film (24) comprises a plurality contiguous monolayers (71a-c) of metal atoms located on the surface of the substrate material (18).

15. A semiconductor device according to claim 9, wherein the barrier film (24) comprises a plurality of contiguous monolayers comprising two or more different types of metal atoms selected from the group consisting of barium atoms, strontium atoms, cesium atoms, and rubidium atoms.

16. A semiconductor device according to claim 9, wherein said barrier film (24) is a single monolayer attached to said surface of the substrate material (18).

17. A semiconductor device according to claim 9, in which said substrate material (18) is a semiconductor.

18. A semiconductor device according to claim 9, in which said substrate material (18) is a silicon semiconductor.

19. A semiconductor device according to claim 9, in which said substrate material (18) is an insulating material.

20. A semiconductor device according to claim 9, in which said substrate material (18) is silicon oxide.

21. A semiconductor device according to claim 9, in which the conductor (22) is a metal.

22. A semiconductor device according to claim 9, in which the conductor (22) comprises copper.

23. A process for making a semiconductor device characterized by the steps of:

forming, on a surface (51) of a substrate material (52), a barrier film (54) having a monolayer of metal atoms immediately adjacent the surface (51) of the substrate material (52); and

depositing a material (22) directly on the barrier film (54).

24. A process for making a semiconductor device characterized by the steps of:

forming, on a surface (51) of a substrate material (52), a barrier film (54) including a layer of elemental metal atoms attached to said surface (51), and where the barrier film has a thickness of less than 100Å; and

depositing a material (22) directly on the barrier film (54).

25. A process according to claim 24, where the substrate material (52) is selected as silicon and the material (22) is selected as a conductor material.

26. A process according to claim 25, wherein the conductor material (22) comprises copper.

27. A process according to claim 24, wherein the barrier film (54) has a thickness of not more than approximately 20Å.

28. A process according to claim 24, wherein the barrier film (54) has a thickness of not more than approximately 5Å.

29. A process according to claim 24, wherein the barrier film (54) comprises one or more monolayers of metal atoms.

30. A process according to claim 24, wherein said step of forming said barrier film (54) comprises sequentially forming a plurality of contiguous monolayers (71a-c) of metal atoms on said surface (51) of said substrate material (52).

31. A process according to claim 24, in which the step of forming the barrier film (54) comprises depositing a monolayer precursor compound (50) on the substrate (52) by molecular beam epitaxy, and then annealing the monolayer precursor compound to form a monolayer (54) of metal atoms on the surface (51) of the substrate (52).

32. A process according to claim 31, wherein the precursor compound (50) is a metal halide.

33. A process according to claim 31, wherein the precursor compound (50) includes a Group I metal halide.

34. A process according to claim 31, wherein the precursor compound (50) includes a Group II metal halide.

35. A process according to claim 31, wherein the precursor compound (50) is a metal halide selected from one or more of BaF_2, $BaCl_2$, SrF_2, $SrCl_2$, CsF, CsCl, RbF, and RbCl.

36. A process according to claim 31, wherein the depositing and annealing steps are repeated one or more times to form a plurality of contiguous monolayers (71a-c) on the surface (51) of the substrate (52).

37. A process according to claim 24, in which the step of forming said barrier film (54) comprises depositing a monolayer precursor compound (50) on said substrate (52) by sputtering, and then annealing said monolayer precursor compound (50) to form a monolayer (54) of metal atoms on the surface (51) of the substrate (52).

38. A process according to claim 37, wherein the precursor compound (50) is a metal halide.

39. A process according to claim 37, wherein the precursor compound (50) includes a Group I metal halide.

40. A process according to claim 37, wherein the precursor compound (50) includes a Group II metal halide.

41. A process according to claim 37, wherein the precursor compound (50) is a metal halide selected from one or more of

BaF_2, $BaCl_2$, SrF_2, $SrCl_2$, CsF, CsCl, RbF, and RbCl.

42. A process according to claim 37, wherein the depositing and annealing steps are repeated one or more times to form a plurality of contiguous monolayers (71a-c) on the surface (51) of the substrate (52).

43. A process according to claim 24, in which the step of forming said barrier film (54) comprises depositing a monolayer precursor compound (50) on said substrate (52) by physical vapor deposition, and then annealing said monolayer precursor compound (50) to form a monolayer of metal atoms on the surface (51) of the substrate (52).

44. A process according to claim 24, in which the step of forming said barrier film (54) comprises depositing a monolayer precursor compound (50) on said substrate (52) by a deposition process selected from the group consisting of molecular beam epitaxy and physical vapor deposition, and then chemical etching said monolayer precursor compound (50) to form a monolayer of metal atoms on the surface (51) of the substrate (52).

45. A process according to claim 24, in which the substrate material (52) is a semiconductor material.

46. A process according to claim 24, in which the substrate material (52) is silicon semiconductor.

47. A process according to claim 24, in which the substrate material (52) is an insulating material.

48. A process according to claim 24, in which the substrate material (52) is a silicon oxide.

49. A process according to claim 24, in which the conductor (22) is a metallic conductor.

50. A process according to claim 24, in which the conductor (22) comprises copper.

51. The product of the process as recited in claim 23.

52. The product of the process as recited in claim 24.

FIG. 1

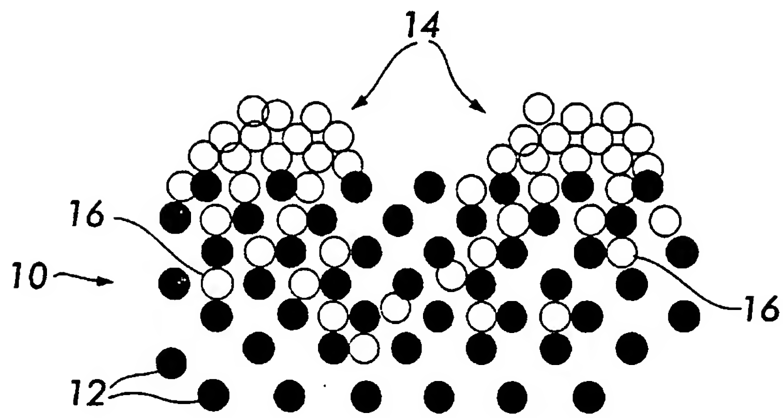


FIG.2

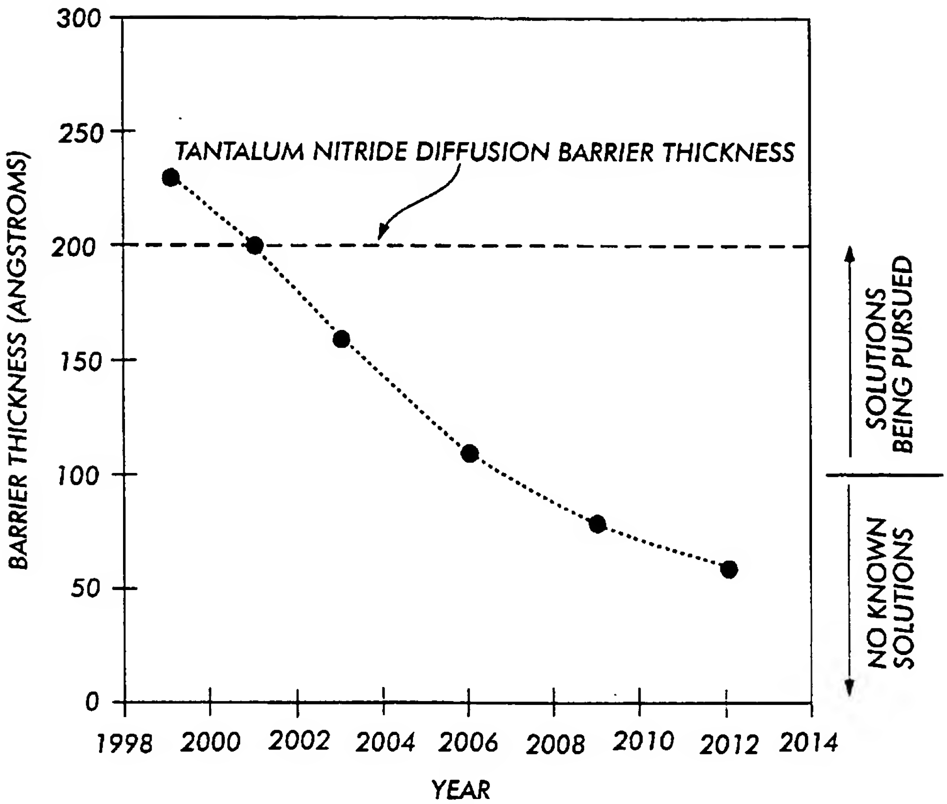

300
250
200
150
100
50
0
BARRIER THICKNESS (ANGSTROMS)
TANTALUM NITRIDE DIFFUSION BARRIER THICKNESS
SOLUTIONS BEING PURSUED
NO KNOWN SOLUTIONS
1998
2000
2002
2004
2006
2008
2010
2012
2014
YEAR

FIG.3

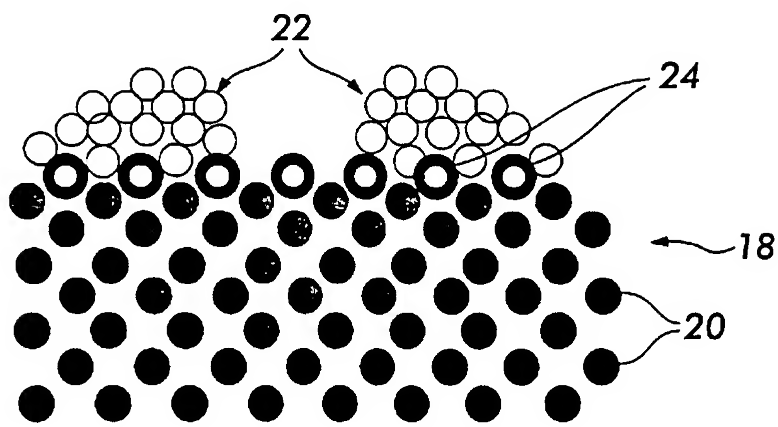


FIG.4

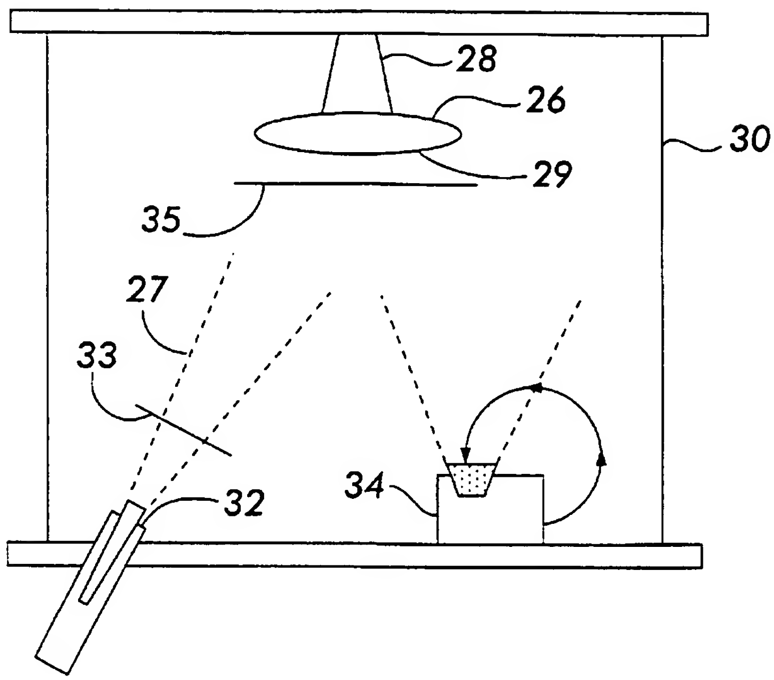


FIG. 5A

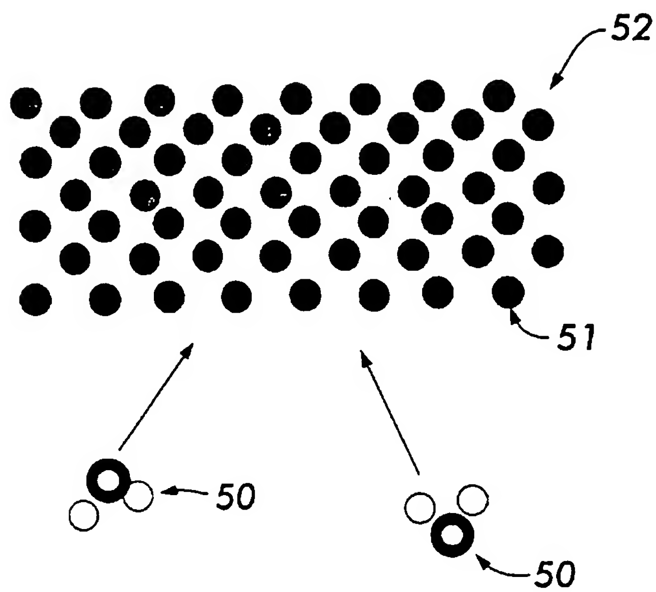


FIG.5B

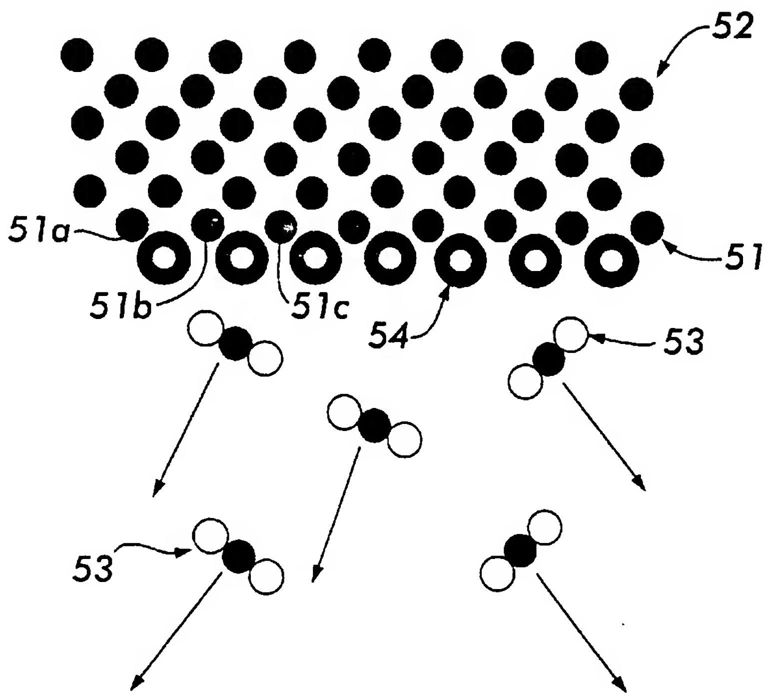


FIG.5C

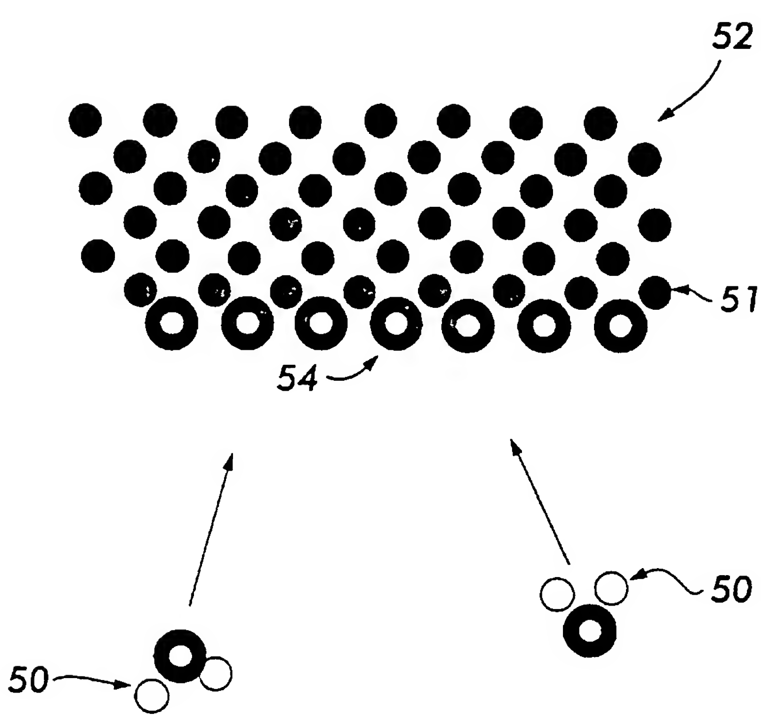


FIG.5D

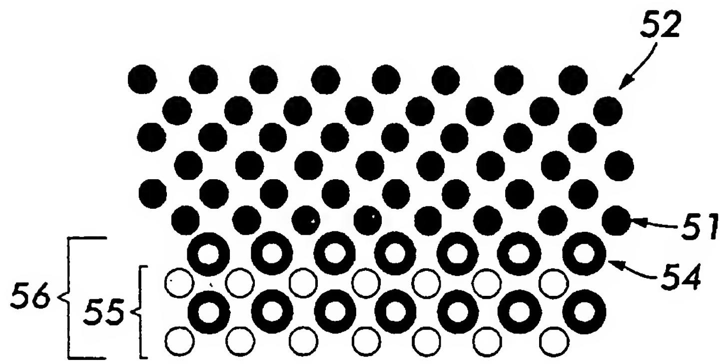


FIG.5E

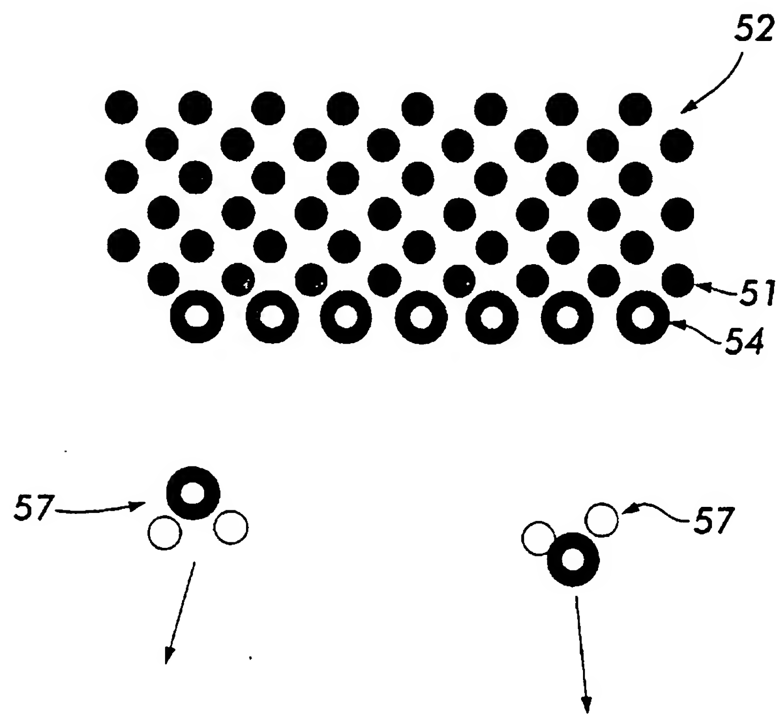


FIG. 6

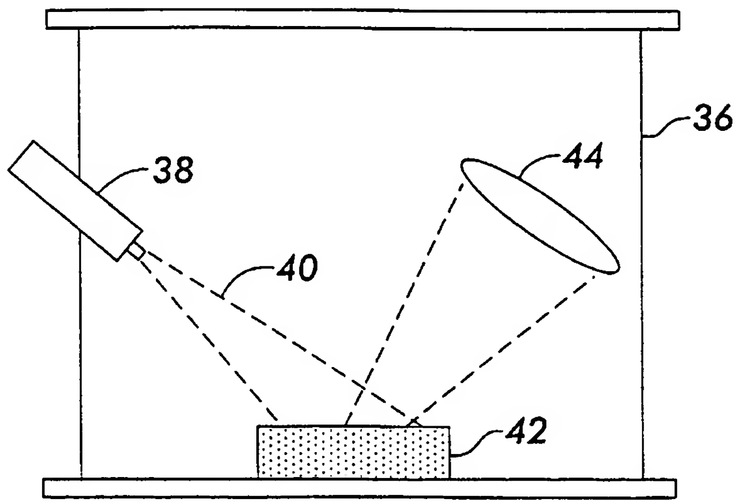


FIG. 7A

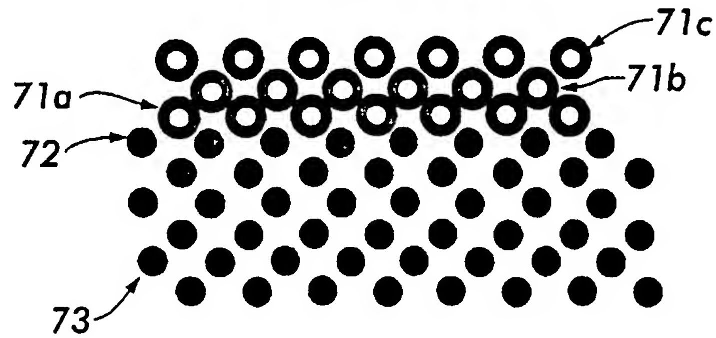


FIG. 7B

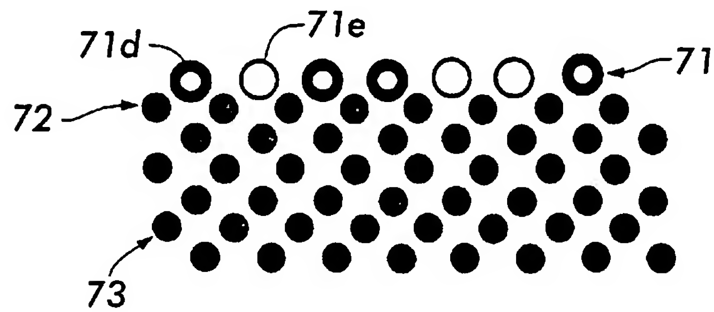


FIG. 7C

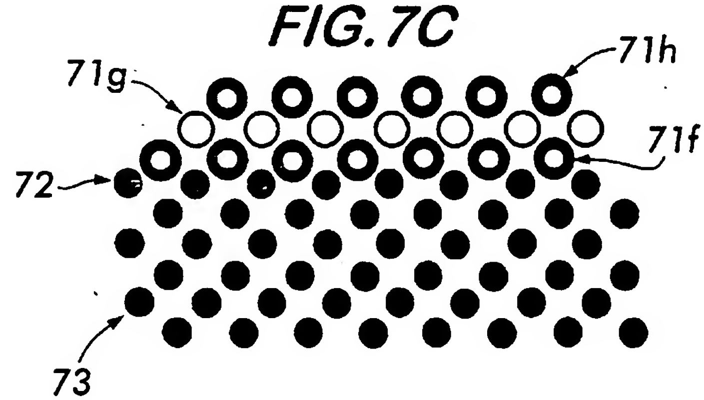
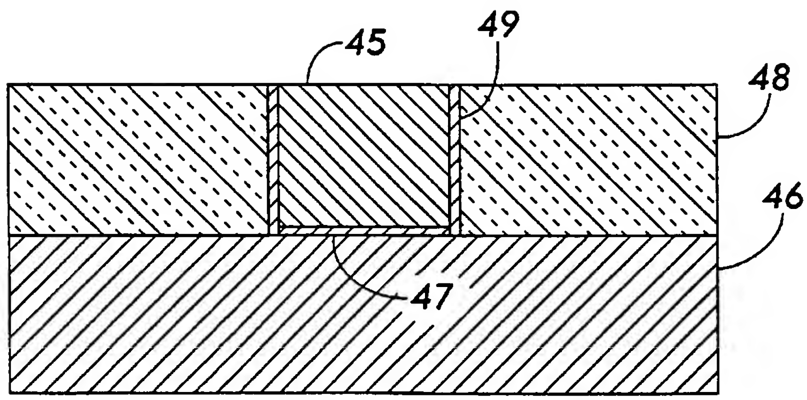


FIG.8



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/16719

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 29/43, 21/441
US CL : 438/687, 643; 257/762,767
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/687, 643; 257/762,767

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 6 310 509 A (NONE) O4 NOVEMBER 1994, (04/11/94) abstract	1, 5, 7, 9,, 14, 17-23, 51
X	EP 0 851 483 A (CHEN et al) 01 JULY 1998, (01/07/98) p.4, lines 55-59; p. 5, lines 1 and 15-19.	1, 2, 5, 7-10, 14, 17-26, 29-30, 45-52
X	US 5,637,533 A (CHOI) 10 JUNE 1997, (10/07/97) col. 2, lines 24-51.	1, 2, 5, 7, 9, 14, 17-23, 51
X	US 5,670,420 A (CHOI) 23 SEPTEMBER 1997, (23/09/97) col. 1, lines 63068; col. 2, lines 10-28.	1, 2, 7, 9, 14, 17-24, 51

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 OCTOBER 1999	17 NOV 1999

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	CARIDAD EVERHART Telephone No. (703) 308-0956

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/16719

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X, P	EP 0 881 673 A (ASHLEY, et al) 02 DECEMBER 1998, (02/12/98) col. 8, lines 55-59; col. 9, lines 1-35.	1, 2, 5, 7-10, 17-24, 45-52
X, P	US 5,824,599 A (SCHACHAM-DIAMAND et al) 20 OCTOBER 1998, (20/10/98) col. 6, lines 35-50	1, 5, 7, 9, 14, 17, 23, 51